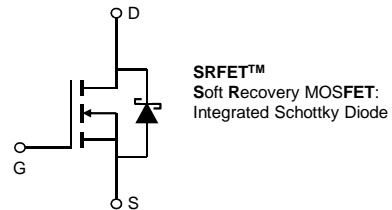


General Description

SRFET™ AO4712 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$, and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications.

Features

V_{DS}	30V
I_D (at $V_{GS}=10V$)	13A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 11m Ω
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	< 14m Ω



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	13
		$T_A=70^\circ\text{C}$	10
Pulsed Drain Current ^C	I_{DM}	68	A
Avalanche Current ^C	I_{AS}, I_{AR}	15	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	11	mJ
Power Dissipation ^B	P_D	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	32	40	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient ^{A, D}		60	75	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	17	24	$^\circ\text{C}/\text{W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =1mA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =125°C			0.5 100	mA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±12V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.1	1.65	2.1	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	68			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =13A T _J =125°C		9 13	11 16	mΩ
		V _{GS} =4.5V, I _D =11A		10.7	14	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =13A		80		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.4	0.7	V
I _S	Maximum Body-Diode Continuous Current				5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	930	1170	1400	pF
C _{oss}	Output Capacitance		90	128	170	pF
C _{riss}	Reverse Transfer Capacitance		45	89	125	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.7	1.4	2.1	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =13A	16	20	24	nC
Q _{g(4.5V)}	Total Gate Charge		7	8.7	10.5	nC
Q _{gs}	Gate Source Charge			3.2		nC
Q _{gd}	Gate Drain Charge			3		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.2Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			2.4		ns
t _{D(off)}	Turn-Off DelayTime			23		ns
t _f	Turn-Off Fall Time			4		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =13A, dI/dt=500A/μs	5.5	7	8.5	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =13A, dI/dt=500A/μs	5	6.5	8	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

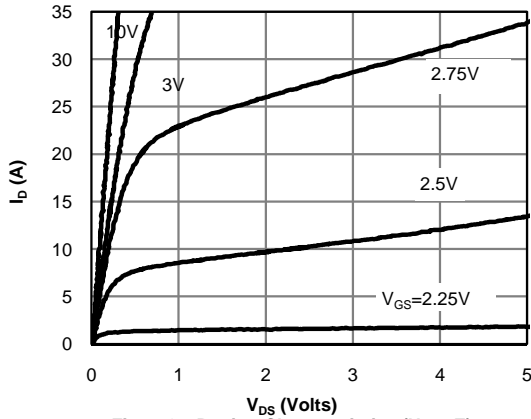


Fig 1: On-Region Characteristics (Note E)

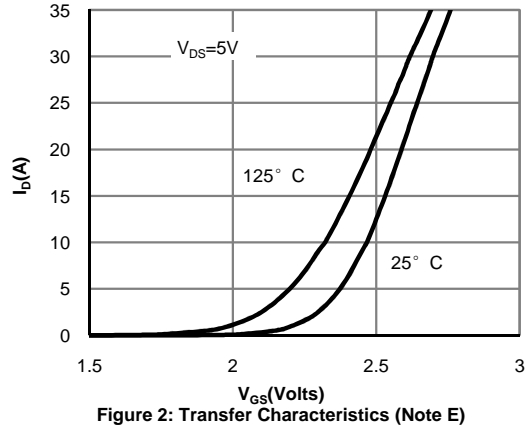


Figure 2: Transfer Characteristics (Note E)

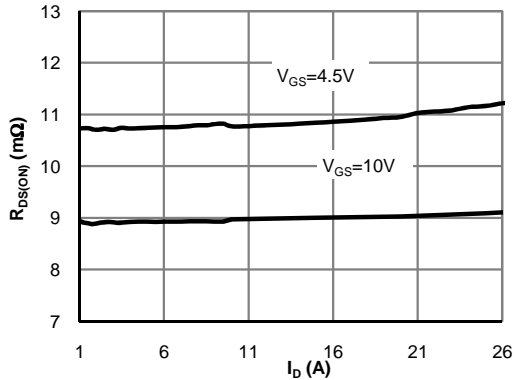


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

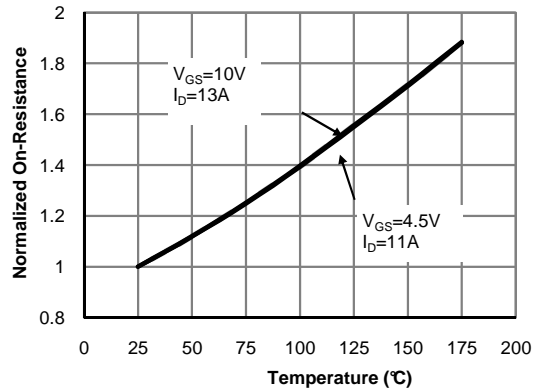


Figure 4: On-Resistance vs. Junction Temperature (Note E)

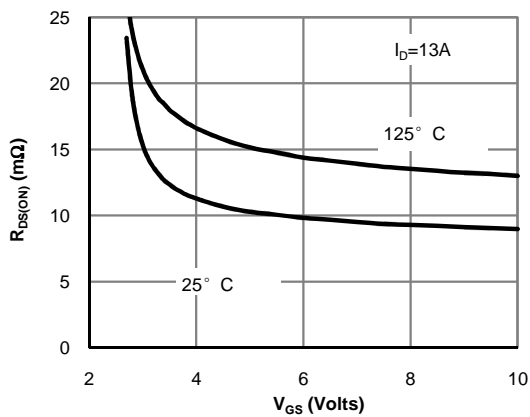


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

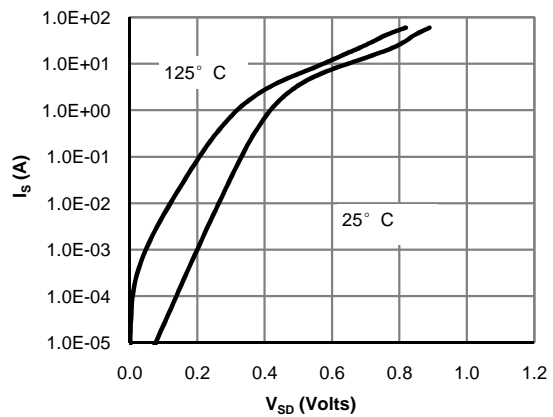


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

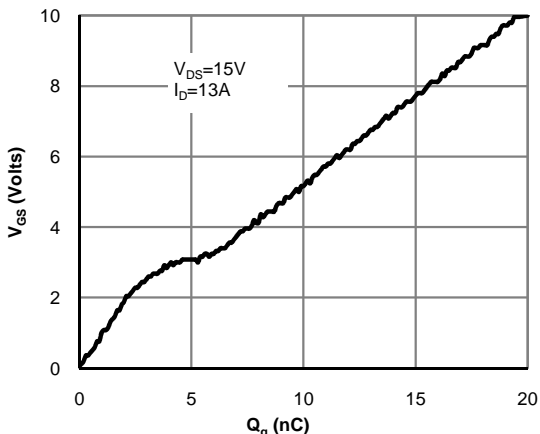


Figure 7: Gate-Charge Characteristics

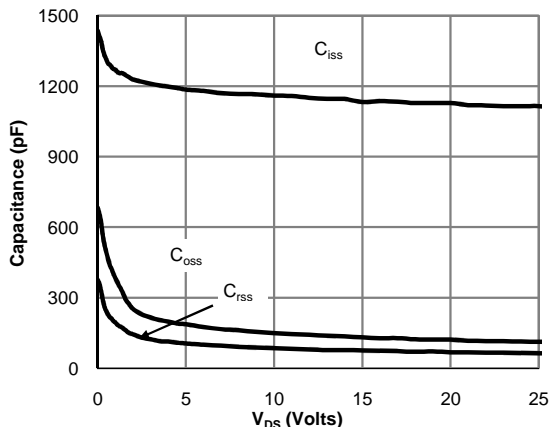


Figure 8: Capacitance Characteristics

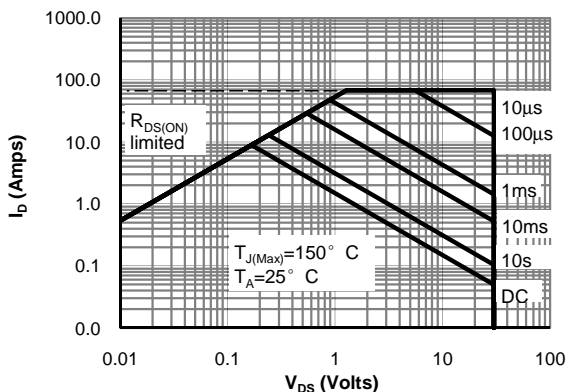


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

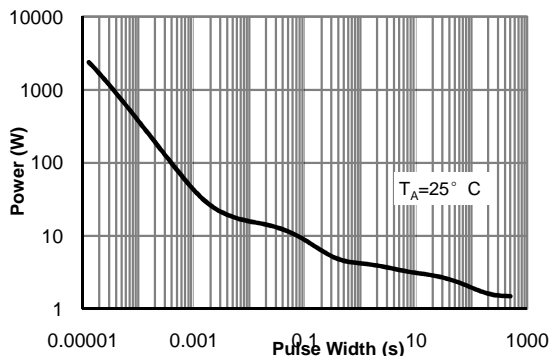


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

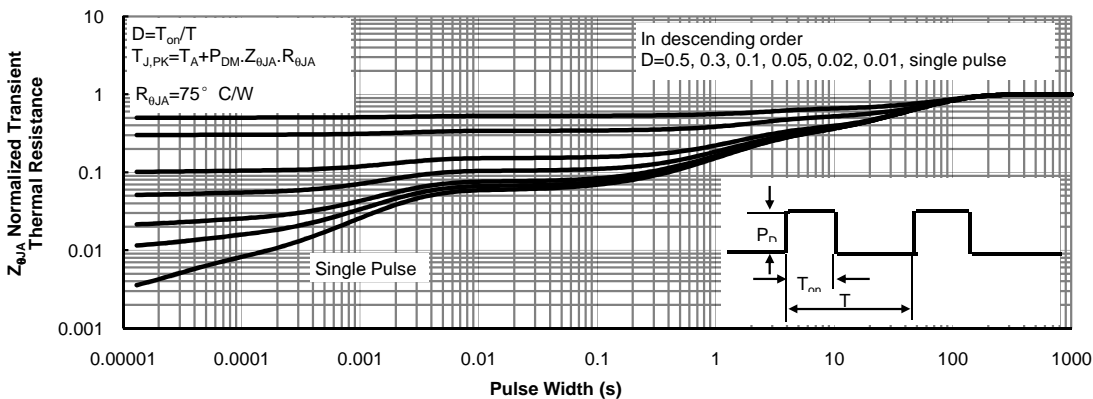


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

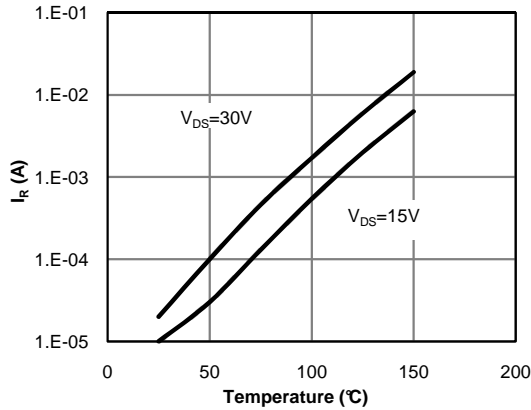


Figure 13: Diode Reverse Leakage Current vs. Junction Temperature

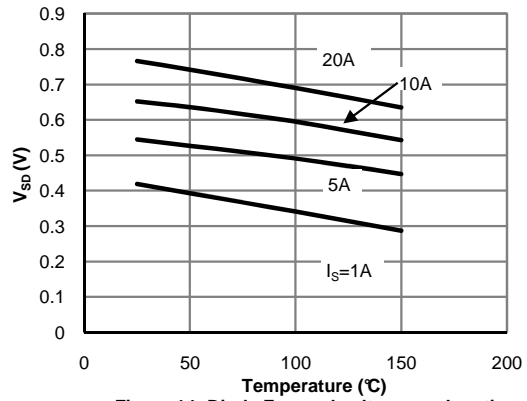


Figure 14: Diode Forward Voltage vs. Junction Temperature

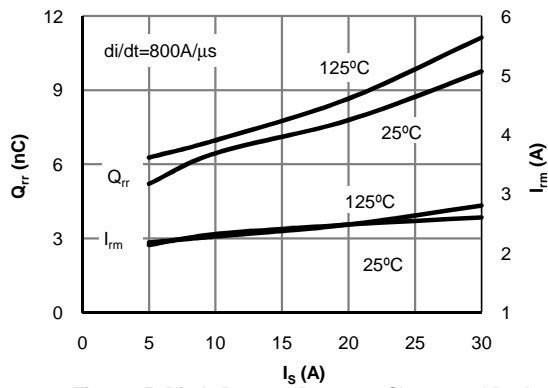


Figure 15: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

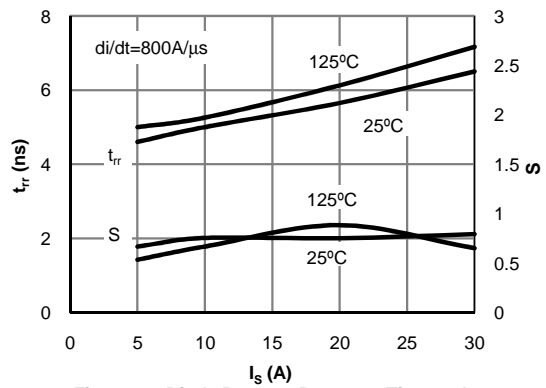


Figure 16: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

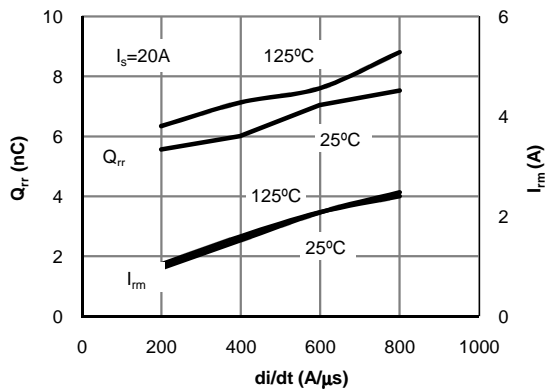


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. di/dt

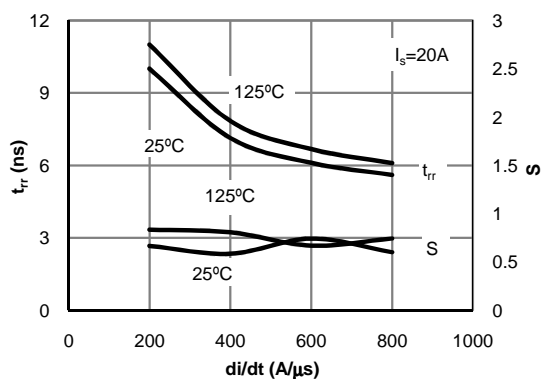
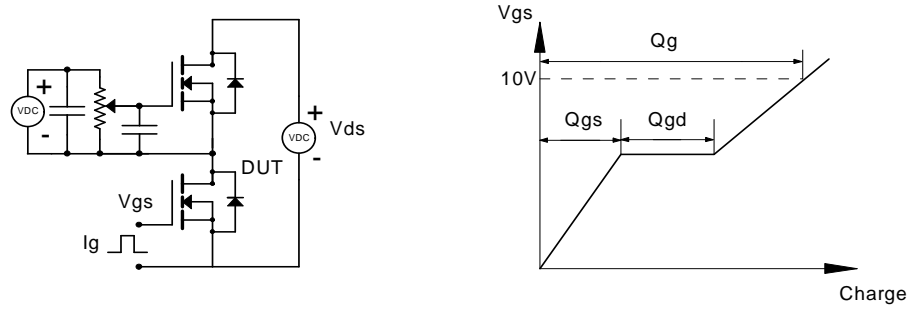
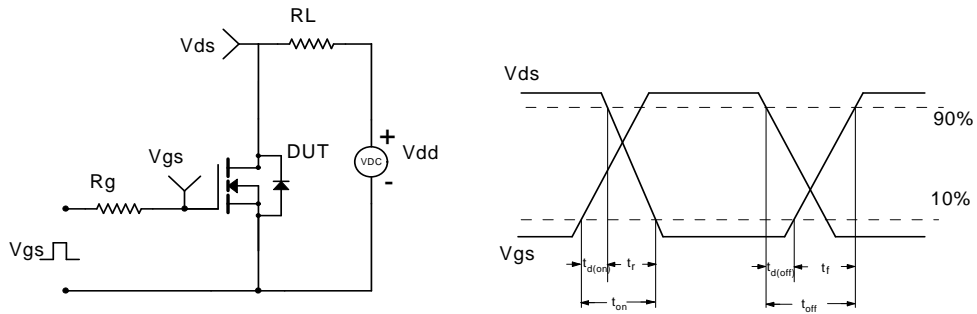


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. di/dt

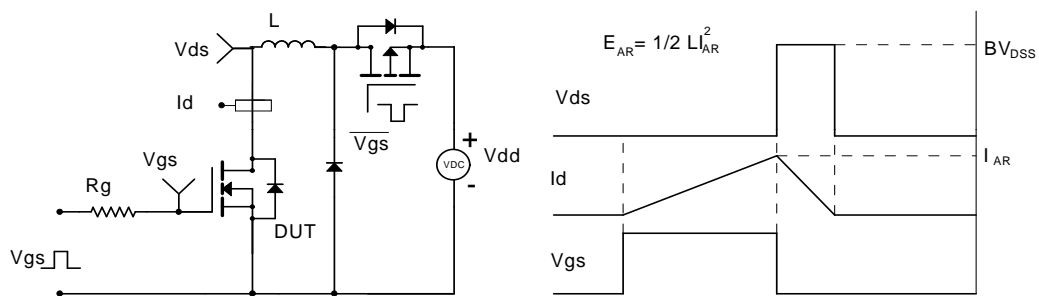
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

